**Case Study 3**

Translate the below into Python code.  
Propose a suitable solution  
  
A diagram of a circuit

AI-generated content may be incorrect.

1. From the Boolean circuits given, obtain the corresponding Boolean expression (one for each circuit a) and b). Be sure showing EACH step marked as a) to j) in both circuits.
2. Create a code in Python that simulates the behavior of each circuit. That is, your code should accept inputs A, B, and C, and print out the corresponding outputs X and Y.
3. Write the truth tables for each circuit and test that your circuits behave as expected.
4. Check that both circuits are equivalent. To do this, use your truth tables in step 3 above.

Boolean Expression

Figure (a)

A = True  
B = True  
C = True

1. A = False
2. C = False
3. A+C = True
4. B = False
5. A + AC + B = False
6. A + C + B = True
7. True

Figure (b)

A = True  
B = True  
C = True

1. B = False
2. B + C = True
3. A + BC = True

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Truth Table - figure a)** | | | | | | |  |  |  |
| A | B | C | a (NOT A) | b (NOT C) | c (A NAND C) | d (NOT B) | e (A + B + AC) | f (A+B+C) | g (A+B+AC OR A+B+C) |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |

Truth tables:

All results from this truth table have been confirmed.

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Truth Table - figure b)** | | | | | | |
| A | | B | C | h (NOT B) | i (C OR B) | J (C/B + A) |
| 1 | | 1 | 1 | 0 | 1 | 1 |
| 1 | | 1 | 0 | 0 | 0 | 0 |
| 1 | | 0 | 1 | 1 | 1 | 1 |
| 1 | | 0 | 0 | 1 | 1 | 1 |
| 0 | | 1 | 1 | 0 | 1 | 0 |
| 0 | | 1 | 0 | 0 | 1 | 0 |
| 0 | | 0 | 1 | 1 | 1 | 0 |
| 0 | | 0 | 0 | 1 | 1 | 0 |

All results for this truth table have been confirmed.

The circuits are not equivalent. Figure a) introduces more detail than figure b). This causes figure b) to have one additional output that results in True.  
This is due to the end of b) expecting 2 inputs to be True, whereas a) is expecting 3 variables that cross more gates.

It can be argued that the circuits are equivalent however figure a) is more complex and thus introduces additional checkpoints, whereas the outlier that is true in b) is a result of the more simple design.